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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/394,302	DEAN ET AL.	
	Examiner	Art Unit	
	Christopher R McGrath	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1-54 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-54 is/are rejected.

7)☒ Claim(s) 2-24 and 40-41 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9/10/1999 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1.0 This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2.0 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 7, line 12 "FIG. 4". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3.0 The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Figure 4a reference character "38", in Figure 5 reference character "49". A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4.0 Claim 22 objected to because of the following informalities: On line 1 "wherein said circuit **comprises comparing**". Appropriate correction is required.

While reviewing the application the examiner has interpreted the claim as "wherein said circuit comprises ***a means for*** comparing".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.0 Claims 2-21 and 23-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2, 6, 7, and 15 recite the limitations where the golden output signal is used to replace defective output signal from a failing chip. The inclusion of these limitations would invalidate the test procedure being performed by always providing a positive result after the initial testing of any given chip. While reviewing the application the examiner has examined the claim and the corresponding dependent claims without these limitations.

Claims 3-21 and 23-24 depend from rejected claim 2 and include all of the limitations of claim 2 thereby rendering these claims indefinite.

5.0 Claims 20, 21, 23, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 20-22 recite the term "golden test result data." The meaning of this term is indefinite and not clarified in the specification.

Claims 23 and 24 depend from rejected claim 21 and include all of the limitations of claim 21 thereby rendering these claims indefinite.

During examination the examiner interpreted the term "golden test result data" to be equivalent to the term "golden output signal" as indicated in claim 20. However, this meaning is contradictory to the meaning indicated in claim 24.

6.0 Claims 40 and 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 40 and 41 recite limitations where the golden output signal is used to replace the output signal of a chip under test. The inclusion of this limitation would invalidate the test procedure being performed by always providing a positive result after the initial testing of any given chip.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 22, 25, 31, 33, 37, 43, 47, and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Paterson U.S. Patent No. 5,566,186.

7.0 Referring to claim 1, the applied reference Paterson discloses a test system for testing a plurality of chips. As per the limitation where the tester comprises "a source of test patterns to stimulate the plurality of chips simultaneously", the applied reference Paterson discloses (column 1, lines 40-45) "The fact that the control device is connectable in parallel to the integrated circuits confers several advantages. For example, more frequent testing of the circuits can be provided than is the case if all the circuits are connected serially and allows a protocol to be provided in which several circuits can be tested simultaneously." With respect to the limitation

where the tester further comprises a "golden output signal", the applied reference Paterson teaches (column 1, lines 57-63) providing an expected response for testing a number of chips. This expected response would act as a golden output signal as defined by the applicant. As per the limitation where the tester further comprises "a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips", the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison circuit local to the chips for comparing the outputs of the chips under test with the golden output signal to determine which chips passed and which chips failed.

8.0 Referring to claim 22, the limitation where the comparison circuit in the tester further comprises a means for "comparing all chip outputs with corresponding golden test result data and then combines results for all comparisons for each chip into a pass of fail signal from each chip", the applied reference Paterson discloses (column 2, lines 56-60 and Figure 2) a means for comparing the outputs and then combining the results of the comparison for each chip into a signal indicating if all the output signals from the chips are the same or different.

9.0 Referring to claim 25, the applied reference Paterson discloses a device for testing integrated circuit chips. As per the limitation where the device comprises "a test circuit for connection to a plurality of integrated circuit chip simultaneously", the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison circuit local to the chips for comparing the outputs of the chips under test with the golden output signal to determine which chips passed and which chips failed. With respect to the limitation where the "test circuit for testing said integrated circuit chips during transport", the applied reference Paterson teaches

(column 1, lines 32-39) a method for testing integrated circuit chip that can be implemented during transport. Conducting the test during transport will merely change the environment in which the test is being conducted and will not require any changes to the testing circuit.

10.0 Referring to claim 31, the limitation where the "test circuit includes a test engine", the applied reference Paterson teaches (column 3, lines 13-16 and Figure 2) "The device also includes a programmable pseudo random binary sequence generator (PRBS) 21. Under the control of the control logic 16, binary sequences of variable length can be generated. For example, different sizes of memory require different length of word to check all of their memory locations." The programmable pseudo random binary sequence generator acts as a test engine under the control of the test control device.

11.0 Referring to claim 33, the limitation where the "test circuit includes a memory", the applied reference Paterson teaches (column 2, lines 3-7) the inclusion of a memory in the test circuit.

11.0 Referring to claim 34, the limitation where the method further comprises "an indicator for identifying which of the integrated circuit chips under test failed said testing", the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison circuit and an error flag generator for identifying which of integrated circuit chips under test failed testing.

12.0 Referring to claim 37, the applied reference Paterson discloses a method for testing a plurality of integrated circuit chips. As per the limitation where the method comprises "providing a source of test patterns to stimulate the plurality of chips simultaneously", the applied reference Paterson discloses (column 1, lines 40-45) "The fact that the control device is connectable in parallel to the integrated circuits confers several advantages. For example, more

frequent testing of the circuits can be provided than is the case if all the circuits are connected serially and allows a protocol to be provided in which several circuits can be tested simultaneously." With respect to the limitation where the method for testing a plurality of chips further comprises "providing a golden output signal", the applied reference Paterson teaches (column 1, lines 57-63) providing an expected response for testing a number of chips. This expected response would act as a golden output signal as defined by the applicant. With respect to the limitation where the method for testing a plurality of chips further comprises "providing a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips", the applied reference Paterson teaches (column 1, lines 57-63) a comparison circuit local to the chips for comparing the outputs of the chips under test with the golden output signal to determine which chips passed and which chips failed.

13.0 Referring to claim 43, the limitation where the "circuit includes a circuit for comparing output signals of said plurality of chips with said golden output signal to determine whether each of said plurality of chips under test passes or fails", the applied reference Paterson teaches (column 2, lines 56-58 and Figure 2) "a mask memory 13 is loaded with an expected return signature and this is then compared with the actual signature by a comparator 14. According to whether the two signatures match, a generator 15 produces an error flag which is sent to the device control logic 16."

14.0 Referring to claim 47, the applied reference Paterson discloses a method for testing integrated circuit chips. With respect to the limitations where the method comprises "transporting said integrated circuit chips" and "testing said integrated circuit chips during said

transporting", the applied reference Paterson teaches (column 1, lines 32-39) a method for testing integrated circuit chip that can be implemented during transport. Conducting the test during transport will merely change the environment in which the test is being conducted and will not require any changes to the testing circuit.

15.0 Referring to claim 49, the limitation where the method further comprises "identifying ones of said integrated circuit chips which failed said testing", the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison circuit and an error flag generator for identifying which of integrated circuit chips under test failed testing.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 10, 20, 26-27, 42, and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga U.S. Patent No. 5,341,314.

16.0 Referring to claim 2, the limitation where the tester further comprises "a test control device, wherein said test control device controls test patterns for testing said plurality of chips in parallel", the applied reference Paterson discloses (column 1, lines 32-39) "a test control device designed to be connected to a plurality of integrated circuits each having an interface provided

for the receipt and transmission of test data for verifying that the respective integrated circuit is functioning correctly, the device having a plurality of sets of ports, one set for each of the circuits to be tested so that the circuits may be connected to the device in parallel to one another."

16.1 With respect to the limitation where the tester further comprises "a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a plurality of chips with each other in response to the test patterns. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

16.2 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the checking circuit in the Bencivenga reference with the tester in the Paterson reference.

17.0 Referring to claim 3, the limitation where the "test control device controls a test engine", the applied reference Paterson teaches (column 3, lines 13-16 and Figure 2) "The device also includes a programmable pseudo random binary sequence generator (PRBS) 21. Under the

control of the control logic 16, binary sequences of variable length can be generated. For example, different sizes of memory require different length of word to check all of their memory locations." The programmable pseudo random binary sequence generator acts as a test engine under the control of the test control device.

18.0 Referring to claim 10, the limitation where the "checking circuit compares each chip with all other connected chips", the applied reference Paterson as altered does not teach this limitation. The Bencivenga reference discloses (column 1, line 63 to column 2, line 14) a checking circuit that compares each chip with all other connected chips. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference could have easily been incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

18.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the checking circuit in the Bencivenga reference with the tester in the Paterson reference.

19.0 Referring to claim 20, the limitation where the tester further comprises "a memory for storing test results for comparison with golden test results", the applied reference Paterson teaches (column 2, lines 3-7) a memory for storing the test results for comparison.

20.0 Referring to claim 26, the limitation where the "test circuit compares said integrated circuit chips with each other", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a plurality of chips with each other in response to the test patterns. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

20.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the test circuit in the Bencivenga reference with the device in the Paterson reference.

21.0 Referring to claim 27, the limitation wherein the "test circuit compares all said integrated circuit chips with all other integrated circuit chips that have not been found to be defective", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a chip under test with all other integrated circuit chips that have not been found to be defective. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the

tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

21.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Bencivenga reference with the Paterson reference as altered to obtain the invention as specified in claim 27.

22.0 Referring to claim 42, the limitation where the "circuit includes a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a plurality of chips with each other in response to the test patterns. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

22.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Bencivenga reference with the Paterson reference to obtain the invention as specified in claim 9.

23.0 Referring to claim 52, the limitation wherein "said testing includes comparing output signals of said integrated circuit chips with each other", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a plurality of chips with each other in response to the test patterns. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if to or more of the chips are indeed electrically different from each other.

23.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Bencivenga reference with the Paterson reference as altered to obtain the invention as specified in claim 52.

24.0 Referring to claim 53, the limitation wherein the "testing includes comparing output signals of one integrated circuit chip with output signals of all other integrated circuit chips that have not been identified as defective", the applied reference Paterson does not teach this limitation. The Bencivenga reference discloses (column 1, line 65 to column 2, line 14) a testing circuit for comparing the output signals from a chip under test with all other integrated circuit chips that have not been identified as defective. The Paterson and Bencivenga references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the

testing circuit in the Bencivenga reference into the tester in the Paterson. The checking circuit in the Bencivenga reference can easily be incorporated into the tester in the Paterson reference since it is a simple logic circuit. The suggestion/motivation for doing so would have been to provide a means for detecting if two or more of the chips are indeed electrically different from each other.

24.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Bencivenga reference with the Paterson reference as altered to obtain the invention as specified in claim 53.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claims 2 and 3 above, and further in view of Hii U.S. Patent No. 6,353,563.

25.0 Referring to claim 4, the limitation where the "test engine comprises a BIST engine", the applied reference Paterson as altered does not disclose this limitation. The Hii reference discloses (column 1, lines 50-56) the inclusion of a BIST engine in an integrated circuit test system. The Paterson and Hii references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the BIST engine in the Hii reference into the tester in the Paterson reference as altered. The BIST engine in the Hii reference could have easily been incorporated into the test circuit in the Paterson reference as altered. The suggestion/motivation

for including a BIST engine in the test system would have been to provide a means for eliminating cross talk among parallel leads that can occasionally cause good devices to fail.

25.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the BIST engine in the Hii reference with the tester in the Patterson reference as altered.

26.0 Referring to claim 5, the limitation where the "test control device controls a memory with stored patterns", the applied reference Paterson as altered does not disclose this limitation. The Hii reference discloses (column 1, lines 50-56) a test control device that that controls a memory with stored patterns. The Paterson and Hii references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. The memory in the Hii reference could have easily been incorporated into the test circuit in the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for eliminating cross talk among parallel leads that can occasionally cause good devices to fail.

26.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the memory in the Hii reference with the tester in the Paterson reference as altered.

Claims 8, 9, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claim 2 above, and further in view of Collins U.S. Patent No. 3,651,315.

27.0 Referring to claim 8, the limitation where the tester further comprises "a power supply for providing a power supply voltage, wherein said test control device controls said power supply voltage to provide stress conditions to chips under test", the applied reference Paterson as altered above does not disclose this limitation. The Collins reference discloses (column 12, line 60 to column 13, line 3) interface adapters that provide a means for controlling power supply voltage to provide stress conditions to the devices under test. The Paterson and Collins references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the interface adapters disclosed by Collins into the test control device of the Paterson reference as altered. The adapters disclosed by Collins could have easily been incorporated into the test control device of the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means to accommodate the various functional requirements of the various chips under test.

27.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Collins reference with Paterson reference as altered to obtain the invention as specified in claim 8.

28.0 Referring to claim 9, the limitation where the tester further comprises "a temperature control for controlling temperature of the plurality of chips, wherein said test control device controls said temperature to provide stress conditions to chips under test", the applied reference Paterson as altered above does not disclose this limitation. The Collins reference discloses (column 13, lines 4-8) interface adapters that provide a means for controlling the temperature of the chips under test in order to provide stress conditions to the devices under test. The Paterson

and Collins references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the interface adapters disclosed by Collins into the test control device of the Paterson reference as altered. The adapters disclosed by Collins could have easily been incorporated into the test control device of the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means to accommodate the various functional requirements of the various chips under test.

28.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Collins reference with the Paterson reference as altered to obtain the invention as specified in claim 9.

29.0 Referring to claim 18, the limitation where the tester further comprises "a register for storing passing or failing chip labels", the applied reference Paterson as altered above does not disclose this limitation. The Collins reference discloses (column 13, lines 4-8) interface adapters that provide a means for controlling the temperature of the chips under test in order to provide stress conditions to the devices under test. The Paterson and Collins references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the interface adapters disclosed by Collins into the test control device of the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means to accommodate the various functional requirements of the various chips under test.

29.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Collins reference with the Paterson reference as altered to obtain the invention as specified in claim 18.

Claims 11-14, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claim 2 above, and further in view of Franke U.S. Patent No. 4,122,995.

30.0 Referring to claim 11, the limitation where the checking circuit comprises an XNOR, the applied reference Paterson as altered does not disclose this limitation. The Franke reference discloses (column 3, lines 43-48 and Fig. 3) a checking circuit that comprises an XNOR. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the checking circuit disclosed in the Franke reference in the Paterson reference as altered. The checking circuit in the Franke reference could have easily been incorporated into the tester in the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

30.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 11.

31.0 Referring to claims 12, it would have been obvious to of included the limitations where the "XNOR is at least n-way, where n is the number of chips that can be tested." Logic circuits with more then two inputs where well known in the art when the invention was made. The Bencivenga reference discloses (column 1, lines 65-66) a checking circuit comprising an XOR circuit that is at least n-way, where n is the number of chips that can be tested. Adding a XNOR that is at least n-way would not change the function of the checking circuit of the Paterson reference as altered in claim 11. An XNOR with at least n inputs could easily be added to the checking circuit.

31.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of added an XNOR is at least n-way to Paterson reference as altered in claim 11 to obtain the invention as specified in claim 12.

32.0 Referring to claims 13, the limitations where the "XNOR is at least n+1 way, wherein data from a golden chip is always included in data arriving at said XNOR", the applied reference Paterson as altered in claims 11 and 12 teaches an XNOR that is at least n+1 way. However, the Paterson reference as altered does not teach the inclusion of data from a golden chip in the data arriving at the XNOR. The Franke reference discloses (column 3, lines 44-48 and FIG. 3) the inclusion of data from a standard unit in the data arriving at the XNOR. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference as altered. The standard unit in the Franke reference could have easily been incorporated into the Paterson

reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit at normal operating speed.

32.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 13.

33.0 Referring to claim 14, the limitation where the "golden output signal is provided by a golden chip", the applied reference Paterson as altered does not disclose this limitation. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a golden output signal from a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference as altered. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit at normal operating speed.

33.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 14.

34.0 Referring to claim 21, the limitation where the "golden test result data are provided by a golden chip", the applied reference Paterson as altered does not disclose this limitation. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing golden test result

data from a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference as altered. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

34.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 21.

35.0 Referring to claim 23, the limitation where circuit comprises an array of 2-way XNOR gates and an OR gate for each chip under test, the applied reference Paterson as altered above does not disclose this limitation. The Franke reference discloses (column 3, lines 43-48 and Fig. 3) a checking circuit that comprises XNOR gates followed by an OR gate. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the checking circuit disclosed in the Franke reference in the Paterson reference as altered. The checking circuit disclosed in the Franke reference could easily be incorporated into the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

35.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 23.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claim 2 above, and further in view of Stoner U.S. Patent No. 4,768,195.

36.0 Referring to claims 16 and 17, the limitations where the tester further comprises "a visible indicator showing passing chips or failing chips" and where the "visible indicator comprises a light", the applied reference Paterson as altered does not teach these limitations. The Stoner reference discloses (column 6, lines 46-51 and Fig. 1) decimals, which are lights that are used as visible indicator to indicate passing or falling chips. The Paterson and Stoner references are analogous art because they are from the same field of endeavor that is the testing integrated circuit chips. When the invention was made, it would have been obvious to of included the decimals disclosed in the Stoner reference in the Paterson reference as altered. The decimals disclosed in the Stoner reference could easily be incorporated into the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for simple means for indicating if an error is detected during a test.

36.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Stoner reference with the Paterson reference as altered to obtain the invention as specified in claims 16 and 17.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claim 2 above, and further in view of Graef U.S. Patent No. 6,037,796.

37.0 Referring to claim 19, the limitation where the tester further comprises "sockets for holding the chips", the applied reference Paterson as altered does not teach this limitation. The Graef reference discloses (column 3, lines 2-4 and Fig. 1) the use of sockets for holding components under test. The Paterson and Graef references are analogous art because they are from the same field of endeavor that is the testing electronic components. When the invention was made, it would have been obvious to of included the sockets disclosed in the Graef reference in the Paterson reference as altered. The sockets disclosed in the Graef reference could easily be incorporated into the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means to easily change the components under test.

37.1 With respect to the limitation where "said sockets, said test control device, said test engine, and said checking circuit are on a single card", the Paterson reference as altered does not disclose this limitation. However, it would have been obvious to of placed the components in the Paterson reference on a single board. Placing the components on a single board would not affect the function of the tester and would not require any change to the circuit layout. The suggestion/motivation for doing so would have been to save space.

37.2 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Graef reference with the Paterson reference as altered to obtain the invention as specified in claim 19.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Collins U.S. Patent No. 3,651,315.

38.0 Referring to claim 30, the limitation where the "test circuit controls said power supply voltage to provide test conditions to chips under test", the applied reference Paterson as altered above does not disclose this limitation. The Collins reference discloses (column 12, line 60 to column 13, line 3) interface adapters that provide a means for controlling power supply voltage to provide stress conditions to the devices under test. The Paterson and Collins references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the interface adapters disclosed by Collins into the test control device of the Paterson reference as altered. The adapters disclosed by Collins could have easily been incorporated into the test control device of the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means to accommodate the various functional requirements of the various chips under test.

38.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Collins reference with Paterson reference as altered to obtain the invention as specified in claim 30.

Claims 32 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Hii U.S. Patent No. 6,353,563.

39.0 Referring to claim 32, the limitation where the "test engine comprises a BIST engine", the applied reference Paterson does not disclose this limitation. The Hii reference discloses (column 1, lines 50-56) the inclusion of a BIST engine in an integrated circuit test system. The Paterson and Hii references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention was made, it would have been obvious to of incorporated the BIST engine in the Hii reference into the tester in the Paterson reference. The BIST engine in the Hii reference could have easily been incorporated into the test circuit in the Paterson reference. The suggestion/motivation for including a BIST engine in the test system would have been to provide a means for eliminating cross talk among parallel leads that can occasionally cause good devices to fail.

39.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the BIST engine in the Hii reference with the tester in the Patterson reference.

40.0 Referring to claim 38, the limitation where the "source of the test patterns comprises a BIST engine or a memory", the applied reference Paterson does not disclose this limitation. The Hii reference discloses (column 1, lines 50-56) the inclusion of a BIST engine and a memory in an integrated circuit test system. The Paterson and Hii references are analogous art because they are from the same field of endeavor that is the testing of integrated circuits. When the invention

was made, it would have been obvious to of incorporated the BIST engine or memory in the Hii reference into the tester in the Paterson reference. The BIST engine or memory in the Hii reference could have easily been incorporated into the test circuit in the Paterson reference. The suggestion/motivation for including a BIST engine in the test system would have been to provide a means for eliminating cross talk among parallel leads that can occasionally cause good devices to fail.

40.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the BIST engine or memory in the Hii reference with the tester in the Patterson reference.

Claims 28, 39, and 44-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Franke U.S. Patent No. 4,122,995.

41.0 Referring to claim 28, the limitation where the "test circuit compares all said integrated circuit chips with a golden chip", the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison circuit for comparing the outputs of the chips under test with a golden output signal. However, the Paterson reference does not disclose the use of a golden chip to provide the golden output signal in the test system. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a golden output signal from a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious

to of included the standard unit disclosed in the Franke reference in the Paterson reference as altered. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

41.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference as altered to obtain the invention as specified in claim 28.

42.0 Referring to claim 39, the limitation where the method further comprises "providing a golden chip wherein in providing step (b) said golden output signal comprises output of said golden chip, and wherein in providing step (a) providing said source of test patterns to stimulate said golden chip and the plurality of chips simultaneously", the applied reference Paterson does not disclose this limitation. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a golden output signal from a standard unit where the test patterns stimulate the standard chip and the chips under test simultaneously. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

42.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference to obtain the invention as specified in claim 39.

43.0 Referring to claim 44, the limitation where "a golden chip provides said golden output signal", the applied reference Paterson does not disclose this limitation. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a golden output signal from a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

43.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference to obtain the invention as specified in claim 44.

44.0 Referring to claim 45, the applied reference Paterson discloses a method of testing an integrated circuit chip. With respect to the limitation where an output signal from a chip under test is compared with a golden output signal to determine whether a chip under test passes or fails, the applied reference Paterson teaches (column 2, lines 56-60 and Figure 2) a comparison

circuit for comparing the outputs of the chips under test with the golden output signal to determine which chips passed and which chips failed.

44.1 As per the limitation where the method for testing integrated circuit chips further comprises "providing a golden chip", the applied reference Paterson does not disclose this limitation. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

44.2 With respect to the limitation the method for testing integrated circuit chips further comprises "providing a golden chip", the applied reference Paterson does not disclose this limitation. However, the Franke reference discloses (column 2, lines 39-42 and FIG. 1) "An appropriately chosen input signal is then concurrently applied to the inputs of both the unit under test and the standard unit." The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference. The suggestion/motivation for doing so would have

been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

44.3 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference to obtain the invention as specified in claim 45.

45.0 Referring to claim 46, the limitation wherein "providing step (b) said test patterns are provided to a plurality of chips under test simultaneously", the applied reference Paterson teaches (column 1, lines 40-45) "The fact that the control device is connectable in parallel to the integrated circuits confers several advantages. For example, more frequent testing of the circuits can be provided than is the case if all the circuits are connected serially and allows a protocol to be provided in which several circuits can be tested simultaneously."

Claims 29 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson U.S. Patent No. 5,566,186.

46.0 Referring to claim 29, the limitation where the device further comprises "a power supply connected to said test circuit, wherein said power supply is for providing a power supply voltage to said test circuit and to the chips", the applied reference Paterson does not disclose this limitation. However, a power supply such as the one described above is implied in the reference since the test system would require one in order to function.

46.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of included the limitation in the Paterson reference where a power supply

is connected to the test circuit, wherein the power supply is for providing a power supply voltage to said test circuit and to the chips.

47.0 Referring to claim 48, the limitation where the method further comprises "supplying power to a test circuit connected to said integrated circuit chips during said transport", the applied reference Paterson does not disclose this limitation. However, a power supply such as the one described above is implied in the reference since the test system would require one in order to function.

47.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of included the limitation in the Paterson reference where the method further comprises supplying power to a test circuit connected to the integrated circuit chips during transport.

Claims 35 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Tallman U.S. Patent No. 4,773,028.

48.0 Referring to claim 35, the limitation wherein the "indicator comprises a memory", the applied reference Paterson does not teach this limitation. The Tallman reference discloses (column 7, lines 53-64 and column 16, lines 9-21) a History Data Collection Unit, which acts as an indicator for identifying which of the integrated circuit chips failed testing that comprises a memory. The Paterson and Tallman references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the History Data Collection Unit disclosed in the

Tallman reference in the Paterson reference. The History Data Collection Unit in the Tallman reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means store information related to the test for future reference.

48.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Tallman reference with the Paterson reference to obtain the invention as specified in claim 35.

49.0 Referring to claim 50, the limitation wherein "identifying comprises storing results of said testing in a memory", the applied reference Paterson does not teach this limitation. The Tallman reference discloses (column 7, lines 53-64 and column 16, lines 9-21) a History Data Collection Unit, which comprises a memory for storing test results. The Paterson and Tallman references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the History Data Collection Unit disclosed in the Tallman reference in the Paterson reference. The History Data Collection Unit in the Tallman reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means store information related to the test for future reference.

49.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Tallman reference with the Paterson reference to obtain the invention as specified in claim 50.

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Bencivenga as applied to claim 52 above, and further in view of Franke U.S. Patent No. 4,122,995.

50.0 Referring to claim 54, the limitation wherein "said testing includes comparing output signals of said integrated circuit chips with a golden chip", the applied reference Paterson does not teach this limitation. The Franke reference teaches (column 1, line 64 to column 2, line 8) comparing output signals of the integrated circuit chips with a standard unit. The standard unit in the Franke reference acts as a golden chip as defined by the applicant. The Paterson and Franke references are analogous art because they are from the same field of endeavor that is the testing of digital logic output signals. When the invention was made, it would have been obvious to of included the standard unit disclosed in the Franke reference in the Paterson reference. The standard unit in the Franke reference could have easily been incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means for continuously testing a digital circuit or unit at normal operating speed.

50.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Franke reference with the Paterson reference to obtain the invention as specified in claim 54.

Claims 36 and 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Paterson in view of Stoner U.S. Patent No. 4,768,195.

51.0 Referring to claim 36, the limitation where the "indicator comprises a visual indicator", the applied reference Paterson does not teach this limitation. The Stoner reference discloses (column 6, lines 46-51 and Fig. 1) decimals, which are lights that are used as visible indicator to indicate passing or falling chips. The Paterson and Stoner references are analogous art because they are from the same field of endeavor that is the testing integrated circuit chips. When the invention was made, it would have been obvious to of included the decimals disclosed in the Stoner reference in the Paterson reference. The decimals disclosed in the Stoner reference could easily be incorporated into the Paterson reference. The suggestion/motivation for doing so would have been to provide a means for simple means for indicating if an error is detected during a test.

51.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Stoner reference with the Paterson reference to obtain the invention as specified in claim 36.

52.0 Referring to claim 51, the limitation where the tester further comprises "displaying visible indicator of passing or failing chips", the applied reference Paterson does not teach this limitation. The Stoner reference discloses (column 6, lines 46-51 and Fig. 1) decimals, which are lights that are used as visible indicator to indicate passing or falling chips. The Paterson and Stoner references are analogous art because they are from the same field of endeavor that is the testing integrated circuit chips. When the invention was made, it would have been obvious to of included the decimals disclosed in the Stoner reference in the Paterson reference. The decimals disclosed in the Stoner reference could easily be incorporated into the Paterson reference. The

suggestion/motivation for doing so would have been to provide a means for simple means for indicating if an error is detected during a test.

52.1 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to of combined the Stoner reference with the Paterson reference to obtain the invention as specified in claim 51.

Conclusion

53.0 Any inquiry concerning this communication should be directed to Christopher R. McGrath at telephone number (703) 305-4897. The examiner can normally be reached Monday-Friday (7:30-5:00), alternate Fridays off.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, can be reached at (703) 305-9713.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist, whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:
Commissioner of Patents and Trademarks
Washington, DC 20231

Or faxed to:
(703) 746-7239, (for formal communications intended for entry)

Or:
(703) 746-7240, (for informal or draft communications, Please label "PROPOSED" OR "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

NADEEM IQBAL
PRIMARY EXAMINER

Christopher R. McGrath
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